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STALABLY	1
STALAC	3
STALACCS	1
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(L15 AND STAL\$5).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	82

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<u>L18</u>	L15 and stal\$5	82	<u>L18</u>
<u>L17</u>	L16 and stal\$5	118	<u>L17</u>
<u>L16</u>	L14 and scoreboard\$3	146	<u>L16</u>
<u>L15</u>	L14 and l6	129	<u>L15</u>
<u>L14</u>	L13 and (invalid\$8 or valid\$8)	9725	<u>L14</u>
<u>L13</u>	(index\$3 or indices) near12 (entr\$5 or instruction\$1)	24068	<u>L13</u>

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<u>L12</u>	L11 and (invalid\$8 or valid\$8)	129	<u>L12</u>
<u>L11</u>	l6 and (index\$3 or indices) near12 (entr\$5 or instruction\$1)	149	<u>L11</u>
<u>L10</u>	l6 and (index\$3 or indices)	201	<u>L10</u>
<u>L9</u>	l4 and l6	29	<u>L9</u>
<u>L8</u>	l4 and l2	125	<u>L8</u>
<u>L7</u>	(712/217)[CCLS]	487	<u>L7</u>
<u>L6</u>	(712/217)![CCLS]	487	<u>L6</u>

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<u>L5</u>	scoreboard\$3 and entr\$5 near8 (invalid\$8 or valid\$8) near25 (index\$3 or indices)	5	<u>L5</u>
<u>L4</u>	scoreboard\$3 and entr\$5 near8 (invalid\$8 or valid\$8)	229	<u>L4</u>
<u>L3</u>	l1 and (index\$3 or indices)	48	<u>L3</u>

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<u>L2</u>	(712/2-300)[CCLS]	10947	<u>L2</u>
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<u>L1</u>	scoreboard\$3 near12 (invalid\$8 or valid\$8)	127	<u>L1</u>
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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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**1. A fast and accurate scoreboard algorithm for estimating stationary backgrounds in an image sequence**Lai, A.H.S.; Yung, N.H.C.;  
Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on  
Volume 4, 31 May-3 June 1998 Page(s):241 - 244 vol.4[AbstractPlus](#) | Full Text: [PDE\(652 KB\)](#) IEEE CNF**2. The B-&E model for adaptive wormhole routing**Shen, X.; Cheung, Y.S.;  
Parallel and Distributed Processing, 1993. Proceedings of the Fifth IEEE Symposium on  
1-4 Dec. 1993 Page(s):170 - 173[AbstractPlus](#) | Full Text: [PDE\(308 KB\)](#) IEEE CNF**3. Verification of an industrial CC-NUMA server**Mukherjee, R.; Nakayama, Y.; Mima, T.;  
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15  
Conference on VLSI Design. Proceedings.  
7-11 Jan. 2002 Page(s):747 - 752[AbstractPlus](#) | Full Text: [PDE\(274 KB\)](#) IEEE CNF**4. An implementation of scoreboarding mechanism for ARM-based SMT processor**Chang-Yong Heo; Kyu-Baik Choi; In-Pyo Hong; Yong-Surk Lee;  
ASIC, 2003. Proceedings. 5th International Conference on  
Volume 1, 21-24 Oct. 2003 Page(s):443 - 446 Vol.1[AbstractPlus](#) | Full Text: [PDE\(343 KB\)](#) IEEE CNF**5. A strategy for avoiding pipeline interlock delays in a microprocessor**Yoshida, T.; Matsuo, M.; Ueda, T.; Saito, Y.;  
Computer Design: VLSI in Computers and Processors, 1990. ICCD '90. Proceedings., 1990 IEEE International  
17-19 Sept. 1990 Page(s):14 - 19[AbstractPlus](#) | Full Text: [PDE\(500 KB\)](#) IEEE CNF**6. A superscalar RISC processor with pseudo vector processing feature**Shimamura, K.; Tanaka, S.; Shimamura, T.; Hotta, T.; Kamada, E.; Sawamoto, H.; Shimizu, T.; Nakazawa, K  
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International  
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